DATA SHEET

PLUS405-37/-45

Programmable logic sequencers
(16 × 64 × 8)

Product specification

1996 Nov 12

IC13 Data Handbook

Philips
Semiconductors

PHILIPS

Programmable logic sequencers ($16 \times 64 \times 8$)

PLUS405-37/-45

DESCRIPTION

The PLUS405 devices are bipolar, programmable state machines of the Mealy type. Both the AND and the OR array are user-programmable. All 64 AND gates are connected to the 16 external dedicated inputs (I0 - I15) and to the feedback paths of the 8 on-chip State Registers (Q_{P0} - Q_{P7}). Two complement arrays support complex IF-THEN-ELSE state transitions with a single product term (input variables C0, C1).

All state transition terms can include True, False and Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective registers. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the State and Output Registers.

All state (Q_{P0} - Q_{P7}) and output (Q_{F0} - Q_{F7}) registers are edge-triggered, clocked J-K flip-flops, with Asynchronous Preset and Reset options. The PLUS405 architecture provides the added flexibility of the J-K toggle function which is indeterminate on S-R flip-flops. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "1". This feature allows the state machine to be asynchronously initialized to known internal state and output conditions, prior to proceeding through a sequence of state transitions. Upon power-up, all registers are unconditionally preset to "1". If desired, the initialization input pin (INIT) can be converted to an $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) function as an additional user-programmable feature.

Availability of two user-programmable clocks allows the user to design two independently clocked state machine functions consisting of four state and four output bits each.

Order codes are listed in the Ordering Information Table.

FEATURES

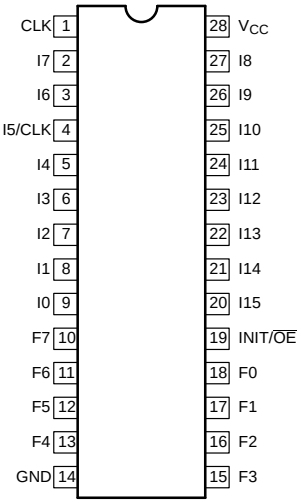
- PLUS405-37
  - f_{MAX} = 37MHz
  - 50MHz clock rate
- PLUS405-45
  - f_{MAX} = 45MHz
  - 58.8MHz clock rate
- Functional superset of PLS105/105A
- Field-programmable (Ti-W fusible link)
- 16 input variables
- 8 output functions
- 64 transition terms
- 8-bit State Register
- 8-bit Output Register
- 2 transition Complement Arrays
- Multiple clocks*
- Programmable Asynchronous Initialization or $\overline{\text{Output Enable}}$
- Power-on preset of all registers to "1"
- "On-chip" diagnostic test mode features for access to state and output registers
- 950mW power dissipation (typ.)
- TTL compatible
- J-K or S-R flip-flop functions
- Automatic "Hold" states
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator contollers
- Security locking systems
- Counters
- Shift registers

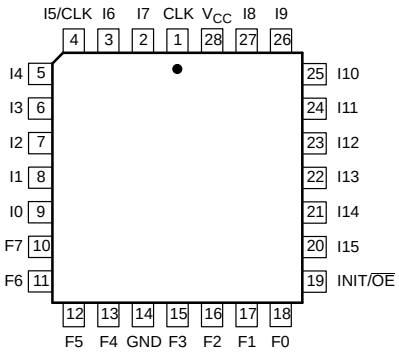
PIN CONFIGURATIONS

N Package



N = Plastic DIP (600mil-wide)

A Package



A = Plastic Leaded Chip Carrier

SP00251

ORDERING INFORMATION

DESCRIPTION	OPERATING FREQUENCY	ORDER CODE	DRAWING NUMBER
28-Pin Plastic DIP (600mil-wide)	45MHz ($t_{IS1} + t_{CKO1}$)	PLUS405–45N	SOT117-2
28-Pin Plastic DIP (600mil-wide)	37MHz ($t_{IS1} + t_{CKO1}$)	PLUS405–37N	SOT117-2
28-Pin Plastic Leaded Chip Carrier	45MHz ($t_{IS1} + t_{CKO1}$)	PLUS405–45A	SOT261-3
28-Pin Plastic Leaded Chip Carrier	37MHz ($t_{IS1} + t_{CKO1}$)	PLUS405–37A	SOT261-3

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK1	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both state and output registers. Pin 1 only clocks P0–3 and F0–3 if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5–9, 26–27 20–22	I0–I4, I7, I6 I8–I9 I13–I15	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of “H” and “L”.	Active-High/Low (H/L)
4	CLK2	**Logic Input/Clock:** A user programmable function:	
		• **Logic Input:** A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock:** A 2nd clock for the State Registers P4–7 and Output Registers F4–7, as above. Note that input buffer I_5 must be deleted from the AND array (i.e., all fuse locations “Don’t Care”) when using Pin 4 as a Clock.	Active-High (H)
23	I12	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I12 is held at +10V, device outputs F0–F7 reflect the contents of State Register bits P0–P7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I11	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I11 is held at +10V, device outputs F0–F7 become direct inputs for State Register bits P0–P7; a Low-to-High transition on the appropriate clock line loads the values on pins F0–F7 into the State Register bits P0–P7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I10	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When I_{10} is held at +10V, device outputs F0–F7 become direct inputs for Output Register bits Q0–Q7; a Low-to-High transition on the appropriate clock line loads the values on pins F0–F7 into the Output Register bits Q0–Q7. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10–13 15–18	F0 – F7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register Bits Q0–Q7, when enabled. When I12 is held at +10V, F0–F7 = (P0–P7). When I11 is held at +10V, F0–F7 become inputs to State Register bits P0–P7. When I10 is held at +10V, F0–F7 become inputs to Output Register bits Q0–Q7.	Active-High (H)
19	INIT/$\overline{OE}$	**Initialization or $\overline{\text{Output Enable}}$ Input:** A user programmable function:	
		• **Initialization:** Provides an asynchronous preset to logic “1” or reset to logic “0” of all State and Output Register bits, determined individually for each register bit through user programming. INIT overrides Clock, and when held High, clocking is inhibited and F0–F7 and P0–P7 are in their initialization state. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after INIT goes Low. See timing definition for t_{NVCK} and t_{VCK}.	Active-High (H)
		• **$\overline{\text{Output Enable}}$:** Provides an output enable function to buffers F0–F7 from the Output Registers.	Active-Low (L)

TRUTH TABLE [1, 2, 3, 4, 5, 6, 7]

V_{CC}	OPTION		I10	I11	I12	CK	J	K	Q_P	Q_F	F
	INIT	$\overline{OE}$									
	H		*	*	*	X	X	X	H/L	H/L	Q_F
	L		+10V	X	X	↑	X	X	Q_P	L	L
	L		+10V	X	X	↑	X	X	Q_P	H	H
	L		X	+10V	X	↑	X	X	L	Q_F	L
	L		X	+10V	X	↑	X	X	H	Q_F	H
	L		X	X	+10V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	*	X	X	X	Q_P	Q_F	Hi-Z
+5V		X	+10V	X	X	↑	X	X	Q_P	L	L
		X	+10V	X	X	↑	X	X	Q_P	H	H
		X	X	+10V	X	↑	X	X	L	Q_F	L
		X	X	+10V	X	↑	X	X	H	Q_F	H
		L	X	X	+10V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	X	X	X	X	X	X	X	X	H	H	

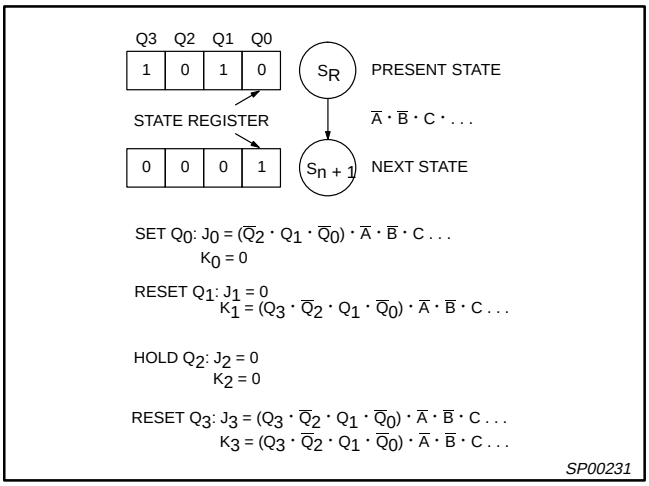
NOTES:
1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   T_n = (C0, C1) (I0, I1, I2, . . .) (P0, P1, . . . P7)
2. Either Initialization (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H or L or +10V
5. X = Don't Care (≤5.5V)
6. H/L implies that either a High or a Low can occur, depending upon user-programmed selection (each State and Output Register individually programmable).
7. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

VIRGIN STATE

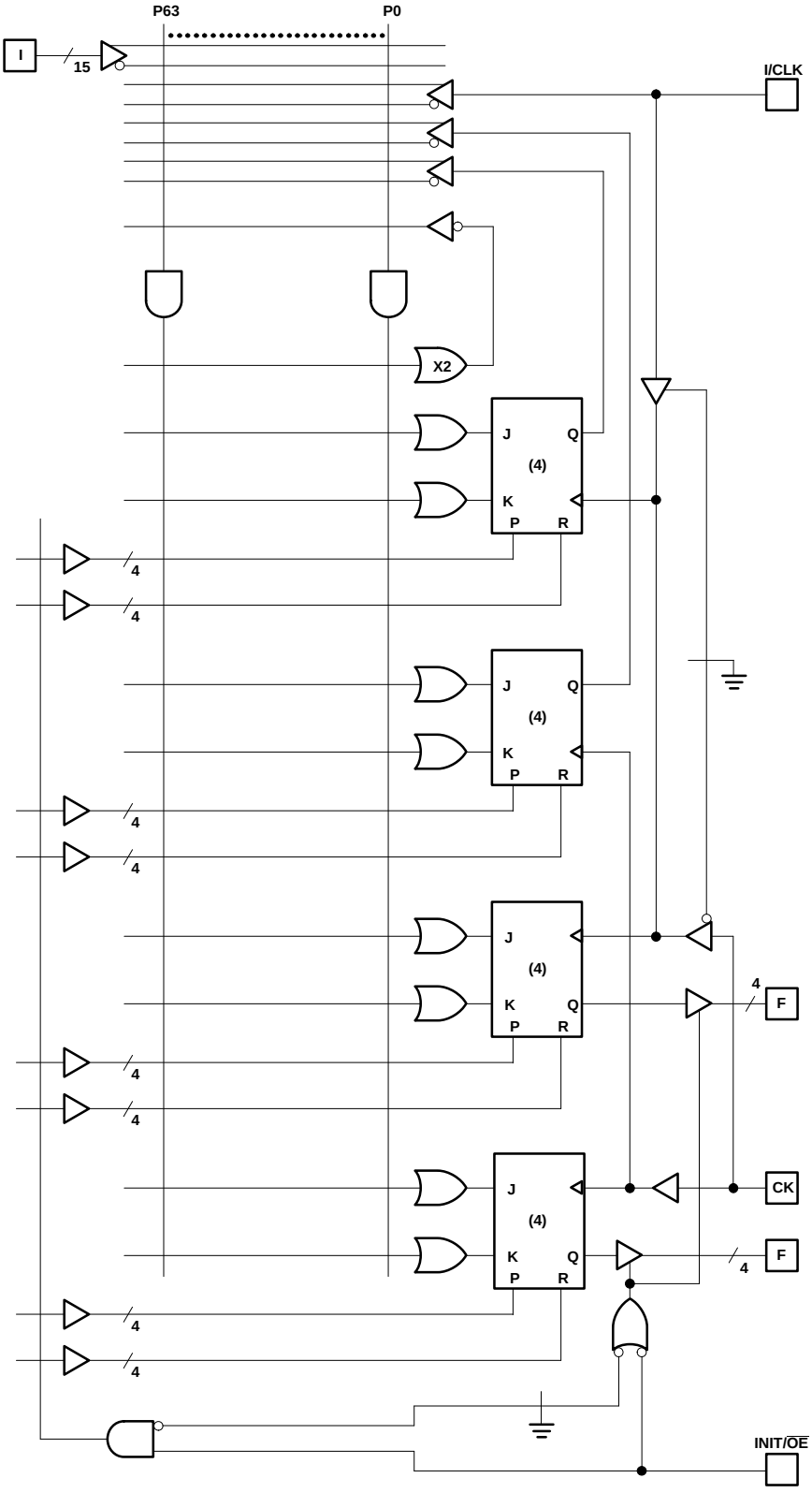
A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$ is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All S/R (or J/K) flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array preprogrammed with a standard test pattern.
5. Clock 2 is inactive.

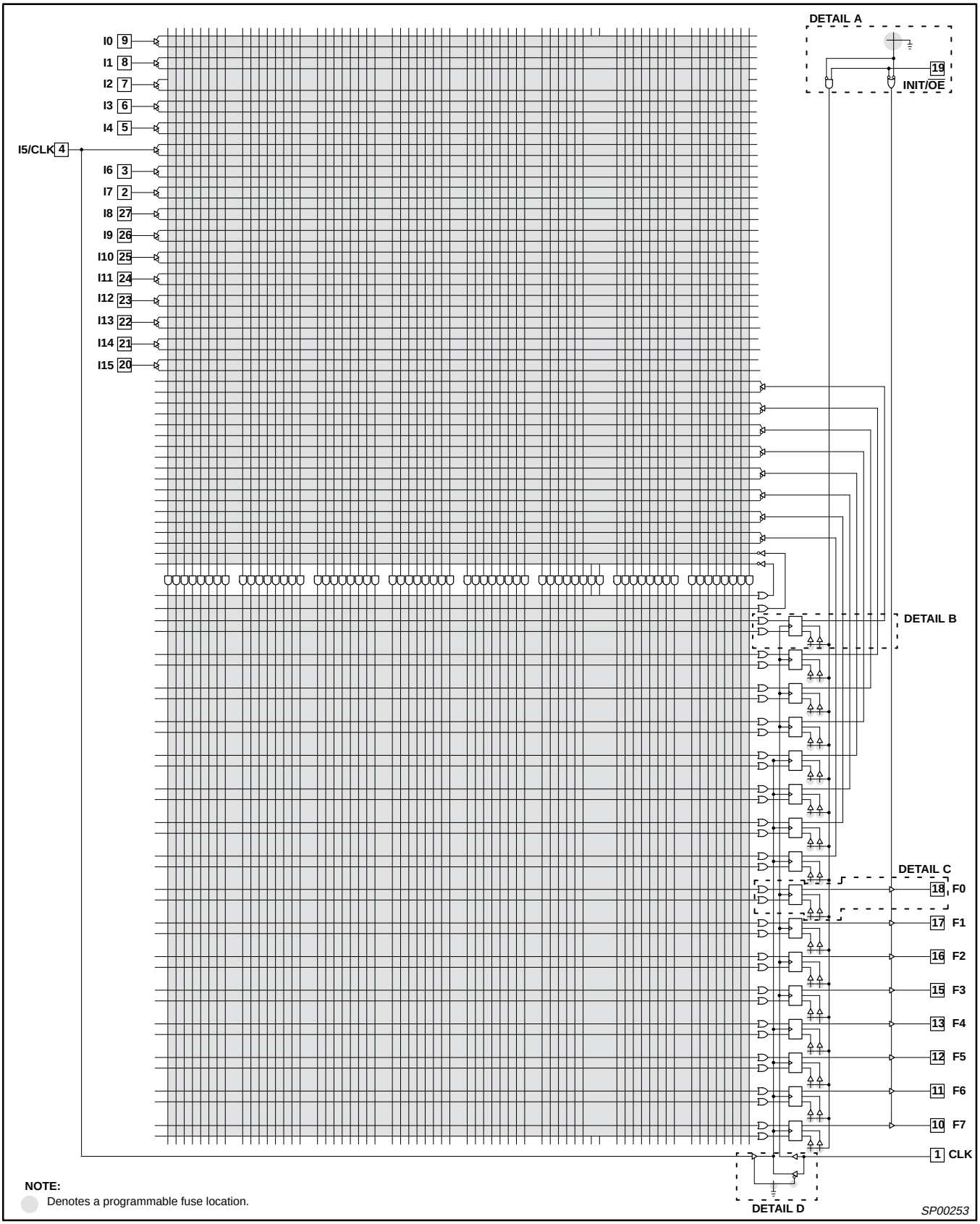
LOGIC FUNCTION



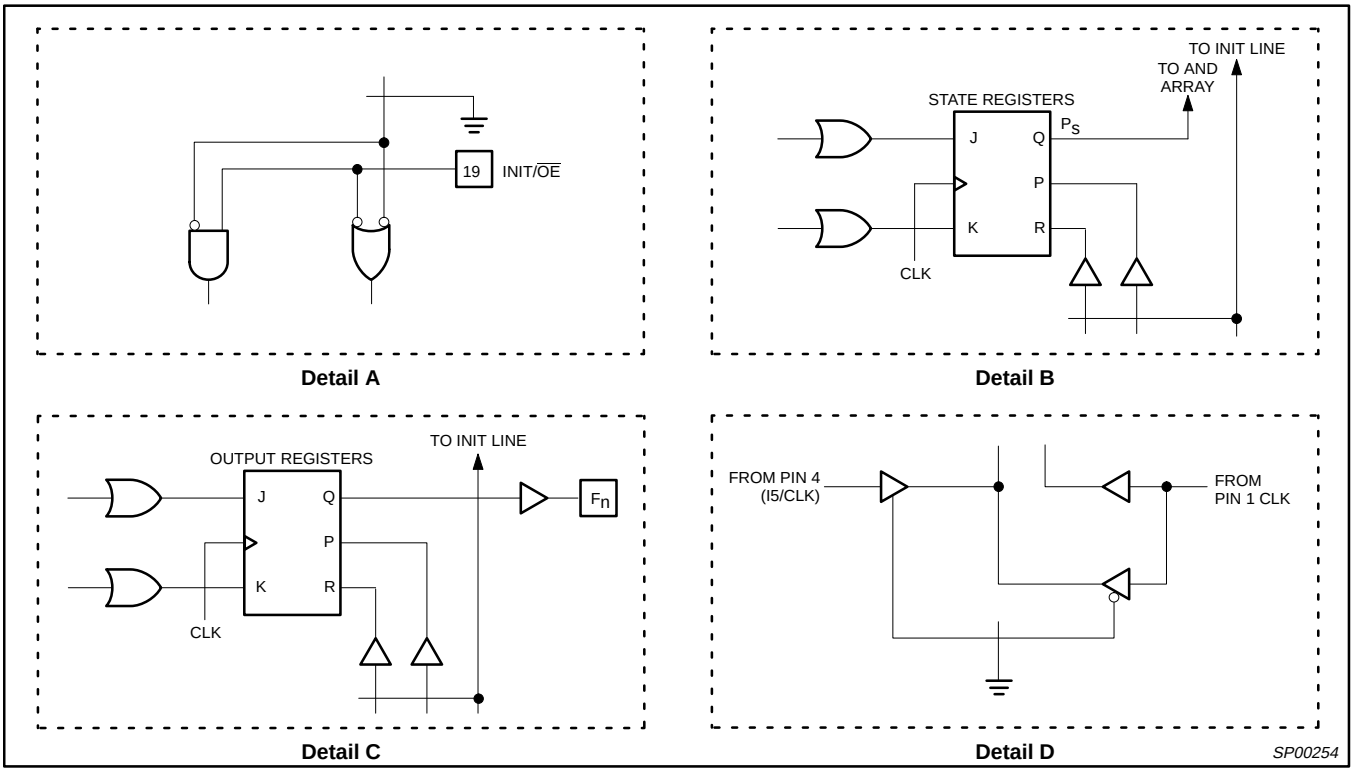
FUNCTIONAL DIAGRAM



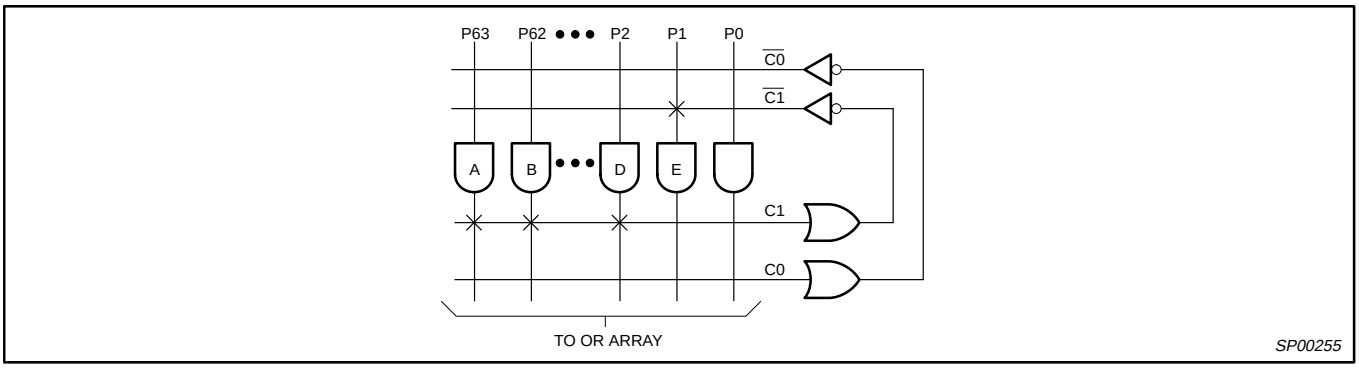
LOGIC DIAGRAM



DETAILS FOR REGISTERS FOR PLUS405



COMPLEMENT ARRAY DETAIL



The Complement Array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The Complement Array is a single OR gate with inputs from the AND array. The output of the Complement Array is inverted and fed back to the AND array (NOR). The output of the array will be Low if any one or more of the AND terms connected to it are active (High). If, however, all the connected terms are inactive (Low), which is a classic unknown state, the output of the Complement Array will be High.

Consider the Product Terms A, B and D that represent defined states. They are also connected to the input of the Complement Array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to Product Term E, which could be used in turn to reset the state machine to a known state. Without the Complement Array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, this approach can be prohibitive, both in terms of time and wasted resources.

Note that the PLUS405 has 2 Complement Arrays which allow the user to design 2 independent Complement functions. This is particularly useful if 2 independent state machines have been implemented on one device.

Note that use of the Complement Array adds an additional delay path through the device. Please refer to the AC Electrical Characteristics for details.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{Sstg}	Storage temperature range	–65 to +150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
V_{OH}	High	V_{CC} = MIN, I_{OH} = –2mA	2.4			V
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{CC} = MAX, V_{IN} = V_{CC}		<1	30	µA
I_{IL}	Low	V_{CC} = MAX, V_{IN} = 0.45V		–20	–250	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{CC} = MAX, V_{OUT} = 2.7V		1	40	µA
		V_{CC} = MAX, V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit [3, 4]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[5]	V_{CC} = MAX		190	225	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{CC} = 5.0V, V_{OUT} = 2.0V		10		pF

NOTES:
1. All typical values are at V_{CC} = 5V. T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Duration of short-circuit should not exceed one second.
5. I_{CC} is measured with the INIT/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS						UNIT
				PLUS405-37			PLUS405-45			
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Pulse width										
t_{CKH1}	Clock High; CLK1 (Pin 1)	CK+	CK–	10	8		8.5	7		ns
t_{CKL1}	Clock Low; CLK1 (Pin 1)	CK–	CK+	10	8		8.5	7		ns
t_{CKP1}	CLK1 Period	CK+	CK+	20	16		17	14		ns
t_{CKH2}	Clock High; CLK2 (Pin 4)	CK+	CK–	10	8		10	8		ns
t_{CKL2}	Clock Low; CLK2 (Pin 4)	CK–	CK+	10	8		10	8		ns
t_{CKP2}	CLK2 Period	CK+	CK+	20	16		20	16		ns
t_{INITH}	Initialization pulse	INIT–	INIT+	15	10		15	8		ns
Setup time										
t_{IS1}	Input	Input ±	CK+	15	12		12	10		ns
t_{IS2}	Input (through Complement Array)	Input ±	CK+	25	20		22	18		ns
t_{VS}	Power-on preset	V_{CC}+	CK–	0	–10		0	–10		ns
t_{VCK}	Clock resume (after Initialization)	INIT–	CK–	0	–5		0	–5		ns
t_{NVCK}	Clock lockout (before Initialization)	CK–	INIT–	15	5		15	5		ns
Hold time										
t_{IH}	Input	CK+	Input ±	0	–5		0	–5		ns
Propagation delay										
t_{CKO1}	Clock1 (Pin 1)	CK1+	Output ±		10	12		8	10	ns
t_{CKO2}	Clock2 (Pin 4)	CK2+	Output ±		12	15		10	12	ns
t_{OE}[2]	Output Enable	OE–	Output –		12	15		12	15	ns
t_{OD}[2]	Output Disable	OE+	Output +		12	15		12	15	ns
t_{INIT}	Initialization	INIT+	Output +		15	20		15	20	ns
t_{PPR}	Power-on Preset	V_{CC} +	Output +		0	10		0	10	ns

Notes on following page

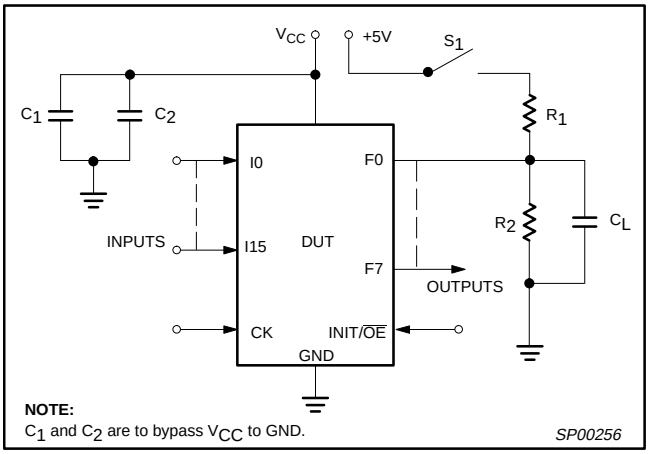
AC ELECTRICAL CHARACTERISTICS (Continued)

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS						UNIT
				PLUS405-37			PLUS405-45			
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Frequency of operation										
f_{MAX1}	CLK1; without Complement Array $\left(\frac{1}{t_{IS1} + t_{CKO1}}\right)$	Input ±	Output ±	37.0	45.5		45.5	55.6		MHz
f_{MAX2}	CLK2; without Complement Array $\left(\frac{1}{t_{IS1} + t_{CKO2}}\right)$	Input ±	Output ±	33.0	41.7		41.7	50.0		MHz
f_{MAX3}	CLK1; with Complement Array $\left(\frac{1}{t_{IS2} + t_{CKO1}}\right)$	Input thru Complement Array ±	Output ±	27.0	33.3		31.3	38.5		MHz
f_{MAX4}	CLK2; with Complement Array $\left(\frac{1}{t_{IS2} + t_{CKO2}}\right)$	Input thru Complement Array ±	Output ±	25.0	31.3		29.4	35.7		MHz
f_{MAX5}	Internal feedback without Complement Array (CLK1 or CLK2) $\left(\frac{1}{t_{CKL} + t_{CKH}}\right)$	Register Output ±	Register Intput ±	50.0	62.5		58.8	72.4		MHz
f_{MAX6}	Internal feedback with Complement Array (CLK1 or CLK2) $\left(\frac{1}{t_{IS2}}\right)$	Register Output thru Complement Array ±	Register Intput ±	40.0	50.0		45.5	55.6		MHz
f_{CLK}	Minimum guaranteed clock frequency	CK +	CK +	50.0	62.5		58.8	72.4		MHZ

NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} – 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. All propagation delays and setup times are measured and specified under worst case conditions.

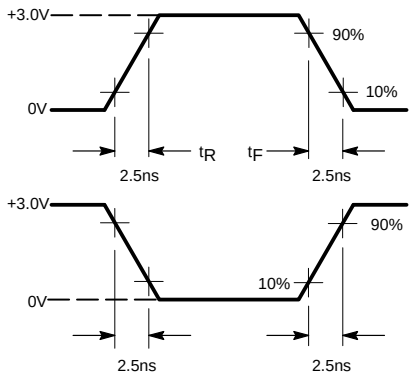
TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

SP00256

VOLTAGE WAVEFORMS

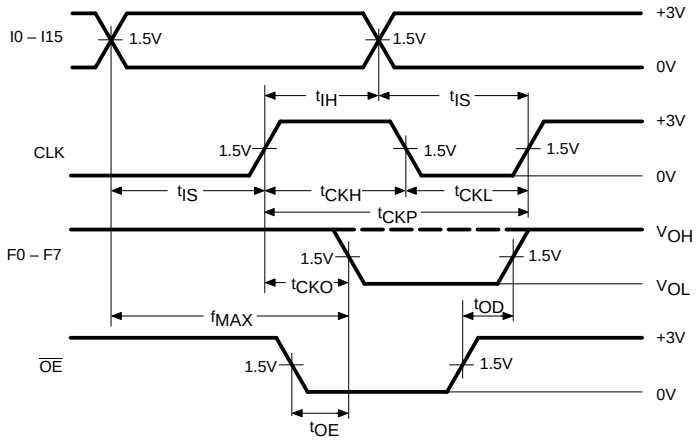


MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

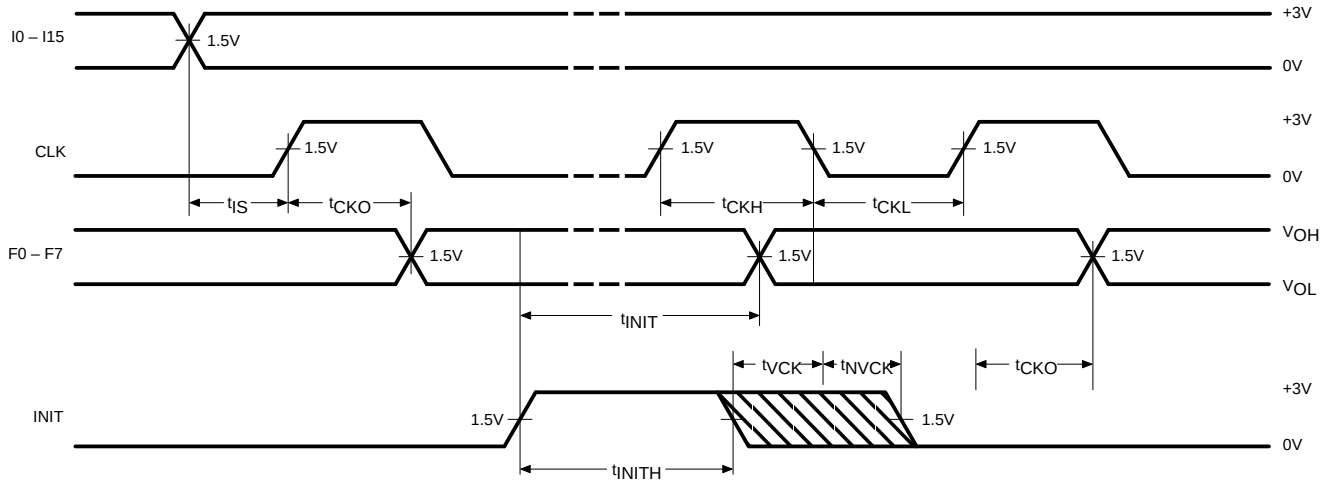
SP00007

TIMING DIAGRAMS



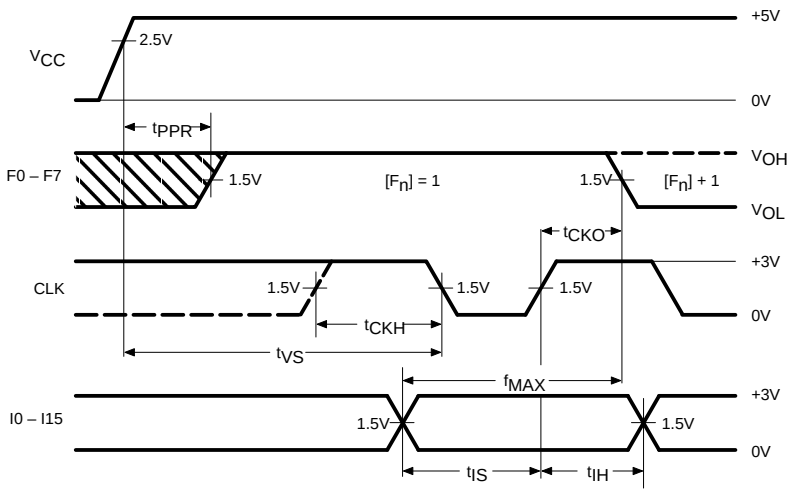
Sequential Mode

SP00257



Asynchronous Initialization

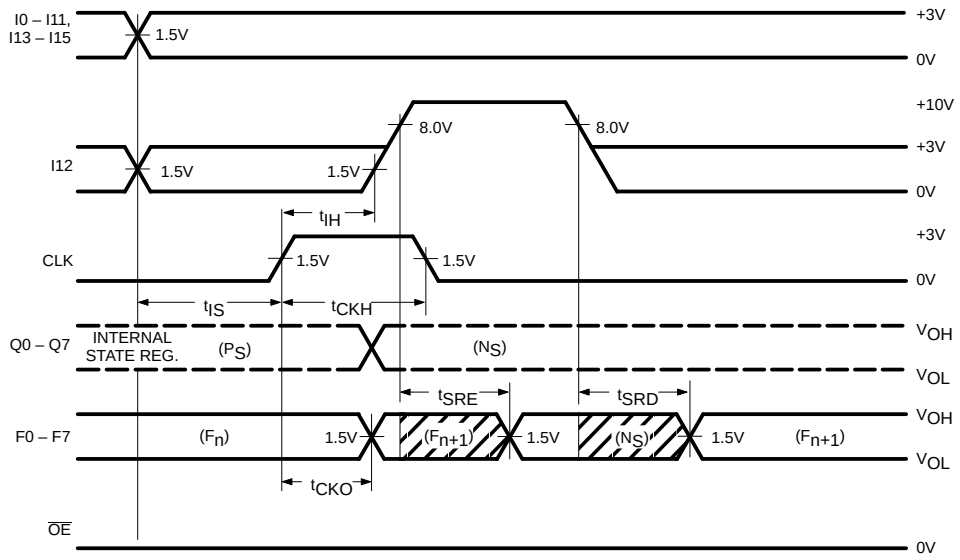
SP00258



Power-On Preset

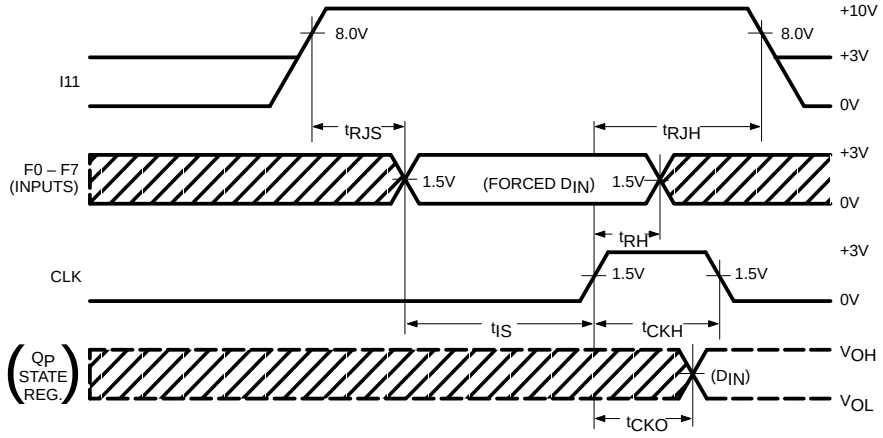
SP00259A

TIMING DIAGRAMS (Continued)



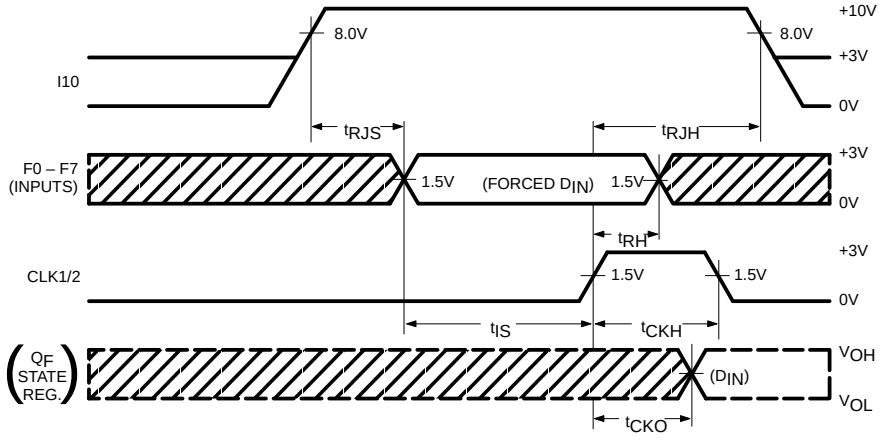
Diagnostic Mode – State Register Outputs

SP00260



Diagnostic Mode – State Register Input Jam

SP00261



Diagnostic Mode—Output Register Input Jam

SP00243

TIMING DEFINITIONS

SYMBOL	PARAMETER
$t_{CKH1, 2}$	Width of input clock pulse.
$t_{CKP1, 2}$	Minimum guaranteed clock period.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
$t_{CKO1, 2}$	Delay between positive transition of Clock and when Outputs become valid (with INIT/$\overline{OE}$ Low).
t_{PPR}	Delay between V_{CC} (after power–on) and when Outputs become preset at “1”.
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{RJH}	Required delay between positive transition of clock, and return of input I10, I11 or I12 from Diagnostic Mode (10V).
$f_{MAX1, 2}$	Minimum guaranteed operating frequency; input to output (CLK1 and CLK2).
$f_{MAX3, 4}$	Minimum guaranteed operating frequency; input through Complement Array, to output (CLK1 and CLK2).
f_{MAX5}	Minimum guaranteed internal operating frequency; with internal feedback from state register to state register.
f_{MAX6}	Minimum guaranteed internal operating frequency with Complement Array, with internal feedback from state register through Complement Array, to state register.
f_{CLK}	Minimum guaranteed clock frequency (register toggle frequency).
$t_{CKL1, 2}$	Interval between clock pulses.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{SRE}	Delay between input I12 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{RJS}	Required delay between inputs I11, I10 or I12 transition to Diagnostic Mode (10V), and when the output pins become available as inputs.
t_{NVCK}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization to guarantee that the clock edge is not detected as a valid negative transition.
t_{INITH}	Width of initialization input pulse.
t_{VS}	Required delay between V_{CC} (after power–on) and negative transition of Clock preceding first reliable clock pulse.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF–state.
t_{INIT}	Delay between positive transition of Initialization and when Outputs become valid.
t_{SRD}	Delay between input I12 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jamming data into State or Output Registers in diagnostic mode.
t_{VCK}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding first reliable clock pulse.

LOGIC PROGRAMMING

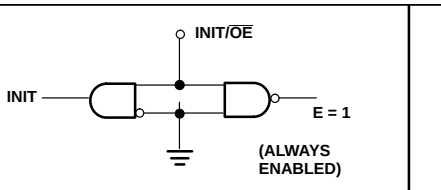
The PLUS405-37/-45 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLUS405-37/-45 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

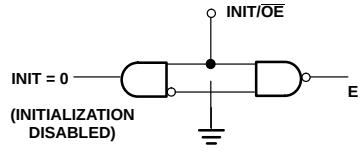
PLUS405-37/-45 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP only.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations is assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

INITIALIZATION/$\overline{OE}$ OPTION – (INIT/$\overline{OE}$)



OPTION	CODE
INITIALIZATION[1]	H

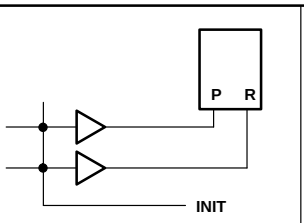


OPTION	CODE
$\overline{OE}$	L

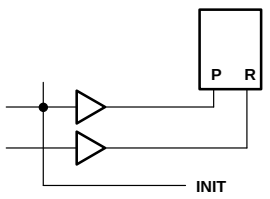
SP00265

PROGRAMMING THE PLUS405:
The PLUS405 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

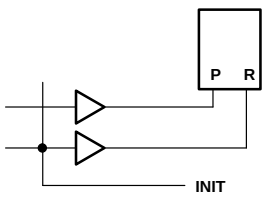
INITIALIZATION OPTION – (INIT)



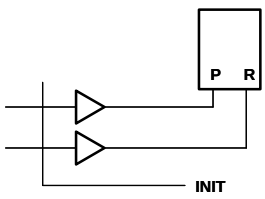
ACTION	CODE
INDETERMINATE[4]	O



ACTION	CODE
PRESET	H



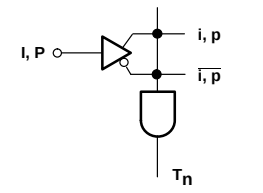
ACTION	CODE
RESET	L



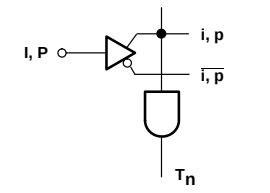
ACTION	CODE
INDETERMINATE[4]	–

SP00266

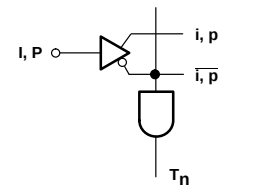
"AND" ARRAY – (I), (P)



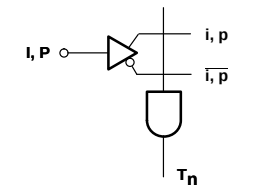
STATE	CODE
INACTIVE[1, 2]	O



STATE	CODE
I, P	H



STATE	CODE
$\overline{I, P}$	L



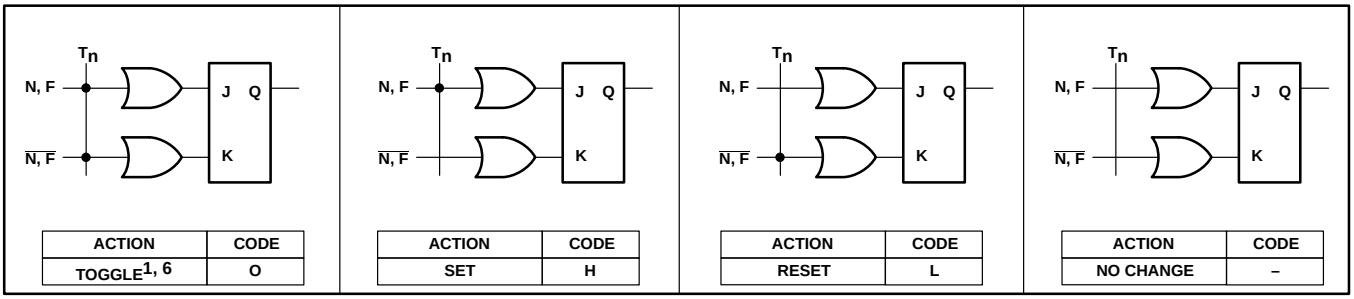
STATE	CODE
DON'T CARE	–

SP00267

Notes are on next page.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

"OR" ARRAY – J-K FUNCTION – (N), (F)



ACTION	CODE
TOGGLE[1, 6]	O

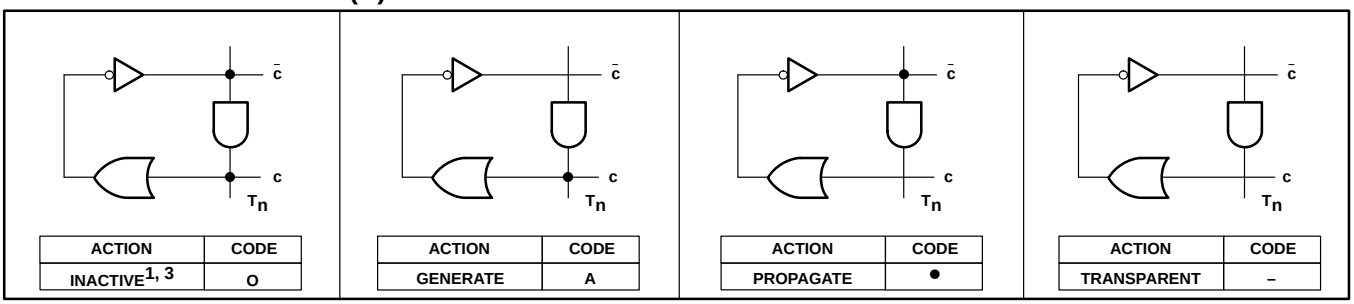
ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

SP00268

"COMPLEMENT" ARRAY – (C)



ACTION	CODE
INACTIVE[1, 3]	O

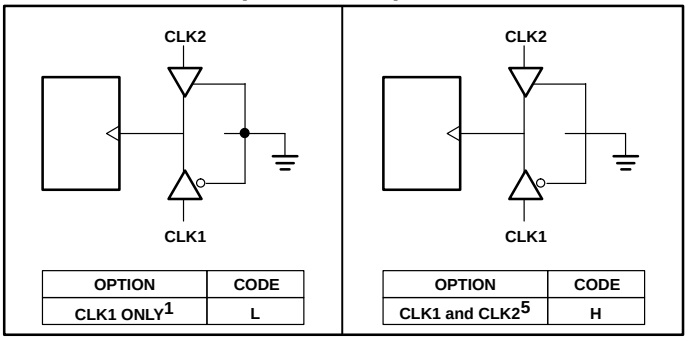
ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	●

ACTION	CODE
TRANSPARENT	–

SP00269

CLOCK OPTION – (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY[1]	L

OPTION	CODE
CLK1 and CLK2[5]	H

SP00270

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4. These states are not allowed when using INITIALIZATION option.
5. Input buffer I5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
6. A single product term cannot drive more than 8 registers by itself when used in TOGGLE mode.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-party Programmer/ Software Support)* of this data handbook for additional information.

PLUS405 PROGRAM TABLE

AND				OR				OPTIONS		
INACTIVE	0	Im, Ps	INACTIVE	0	Cn	INACTIVE OR TOGGLE	0	Ns, Fr	INIT	H	INIT/$\overline{OE}$
I, P	H		GENERATE	A		SET	H		$\overline{OE}$	L	
$\overline{I}$, P	L		PROPAGATE	●		RESET	L		CLK1 ONLY	L	CLK1/CLK2
DON'T CARE	–		TRANSPARENT	–		NO CHANGE	–		CLK1 AND 2	H	

CUSTOMER NAME _____ REV _____ DATE _____

PHILIPS DEVICE # _____ CF (XXXX) _____ PROGRAM TABLE _____

CUSTOMER SYMBOLIZED PART # _____

	CLOCK 1/2	AND																	OR														
		COMP. ARRAY		INPUT (Im)															PRESENT STATE (Ps)								NEXT STATE (Ns)								OUTPUT (Fr)							
		C1	C0	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	P7	P6	P5	P4	P3	P2	P1	P0	N7	N6	N5	N4	N3	N2	N1	N0	F7	F6	F5	F4	F3	F2	F1	F0
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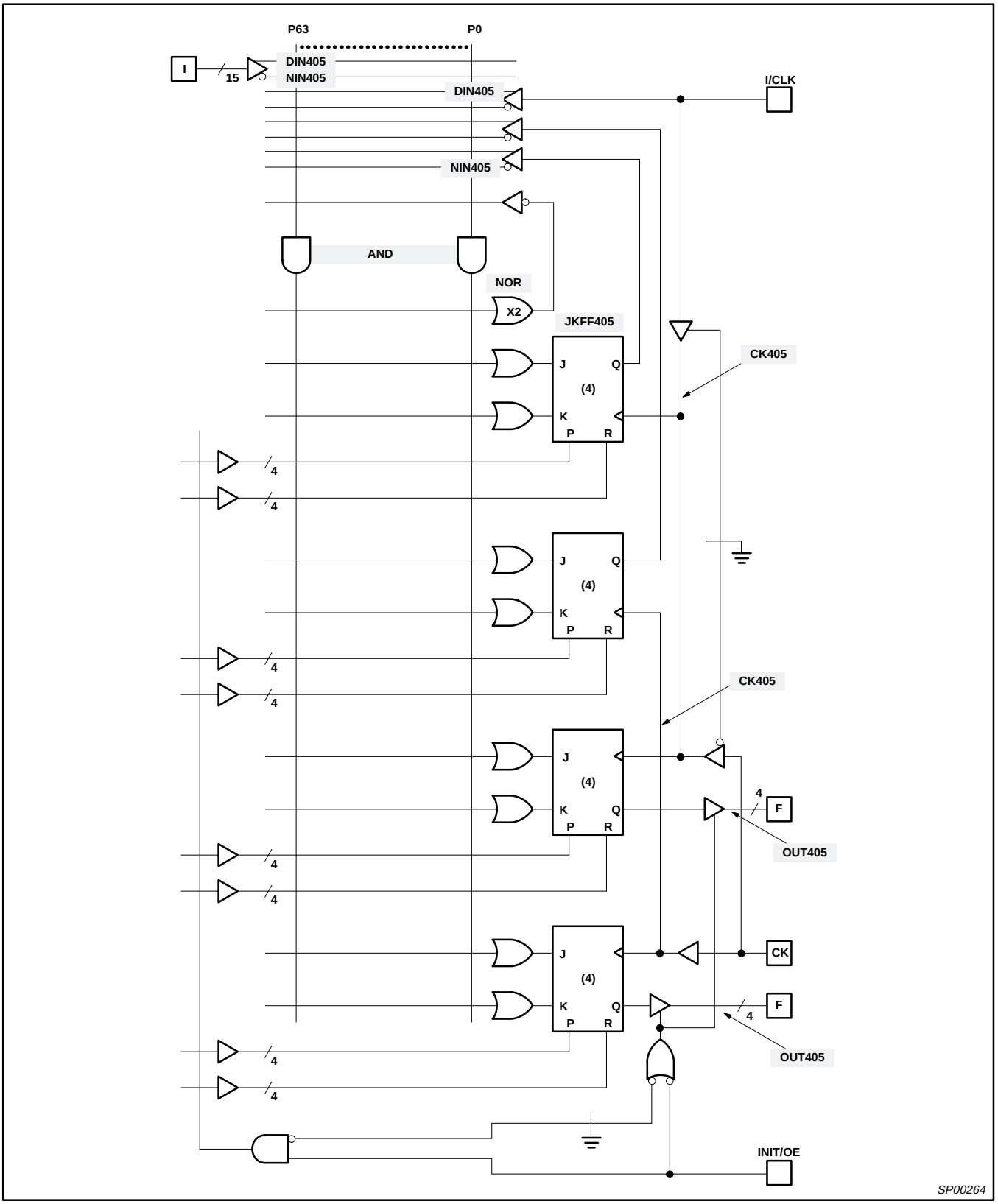
PIN NO.				20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9																10	11	12	13	15	16	17	18
PIN LABELS																																										

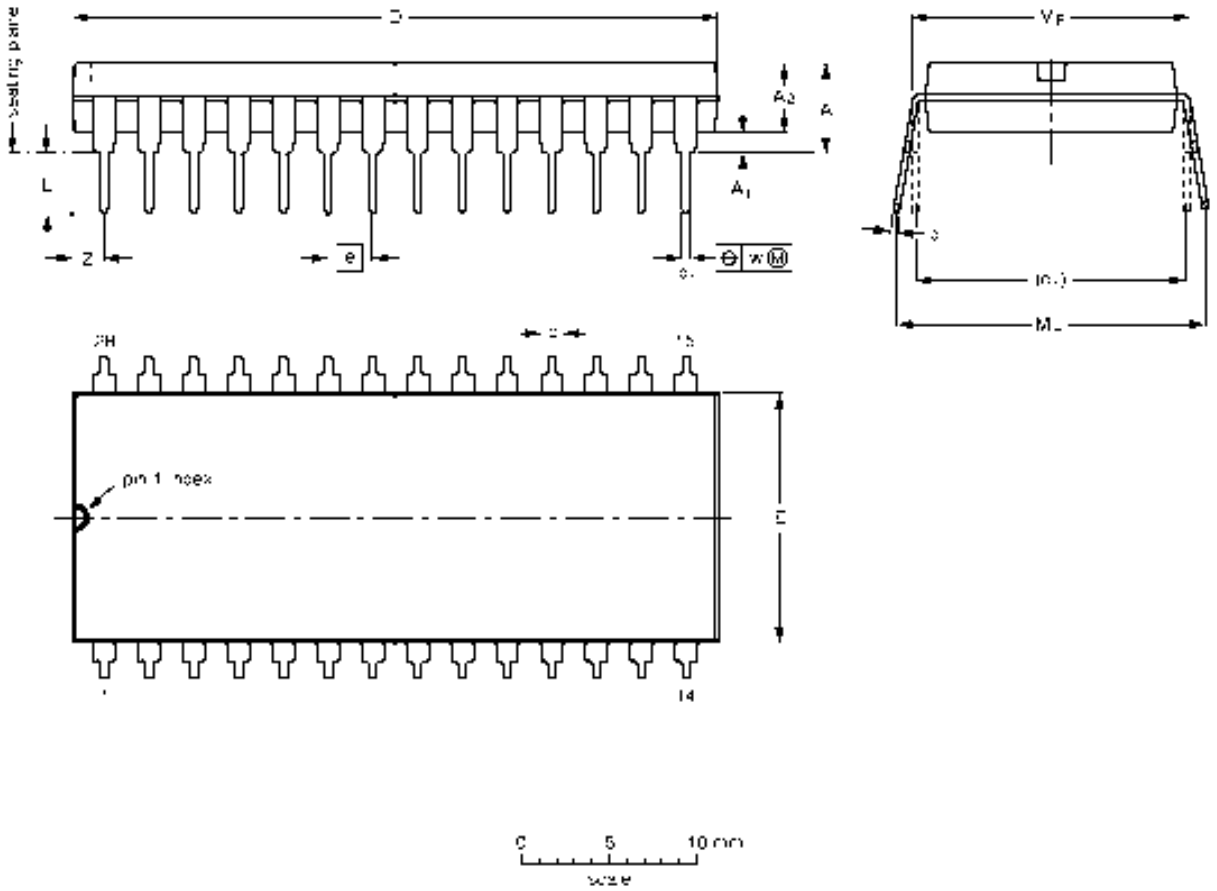
NOTES:
1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the IN/E and H for the clock option, exists in the table, shown BLANK instead for clarity.
2. Unused Cn Im, and Ps bits are normally programmed Don't Care (—).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (—) for maximum speed.

SP00263

SNAP RESOURCE SUMMARY DESIGNATIONS



DIP28: plastic dual in-line package; 28 leads (600 mil); long body **SOT117-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

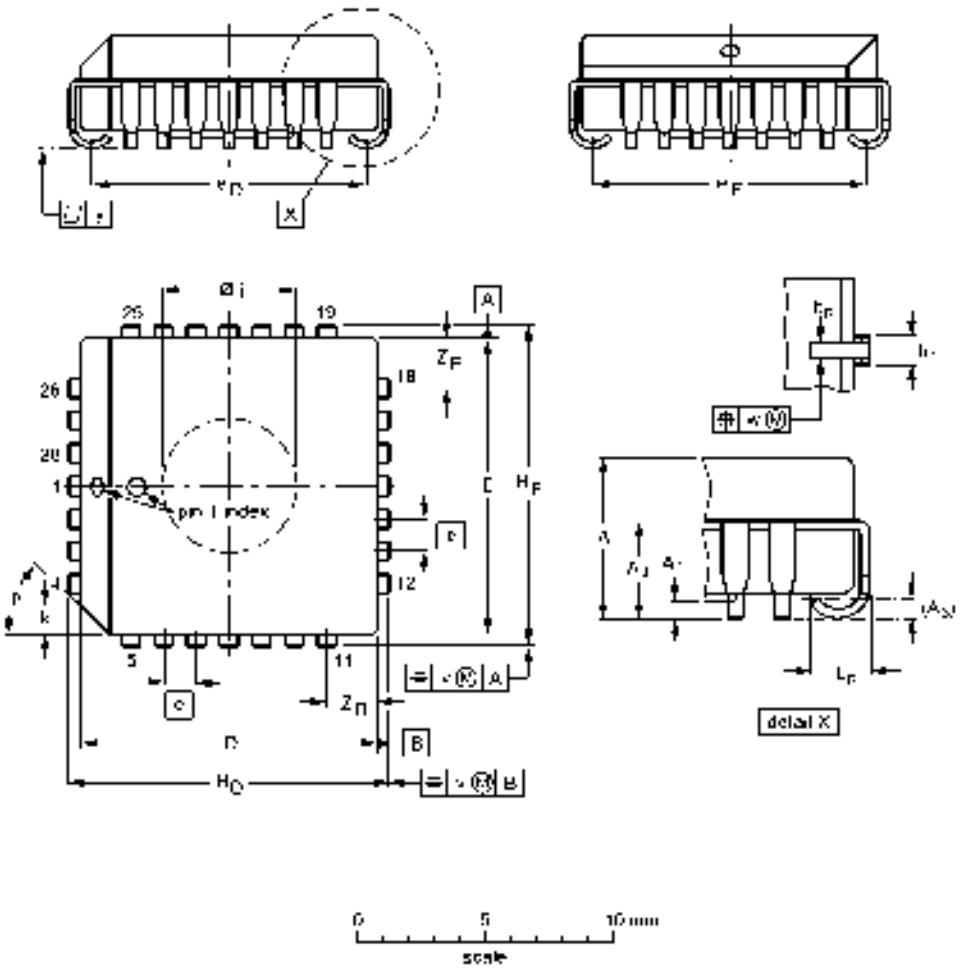
UNIT	A max.	A_1 min.	A_2 max	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	5.00	0.51	3.94	1.53 1.14	0.56 0.43	0.38 0.25	37.60 36.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
inches	0.200	0.020	0.155	0.060 0.045	0.022 0.017	0.015 0.010	1.480 1.455	0.560 0.545	0.100	0.600	0.138 0.120	0.620 0.600	0.695 0.680	0.01	0.083

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-2		MS-011 AB				95-03-11

PLCC28: plastic leaded chip carrer; 28 leads; pedestal **SOT261-3**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_2	A_3 max.	b_p	b_1	D[1]	E[1]	e	e_D	e_E	H_D	H_E	k	k_1	L_p	v	w	y	Z_D[1] max.	Z_E[1] max.	β
mm	4.57 4.19	0.51	3.05	3.66	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.32 12.32	1.22 1.07	3.99 3.84	1.44 1.02	0.18	0.18	0.10	2.05	2.06	45°
inches	0.180 0.165	0.020	0.120	0.144	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.485 0.485	0.048 0.042	0.157 0.151	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT261-3		MO-047AB			95-11-17 03-02-25

Programmable logic sequencers ($16 \times 64 \times 8$)

PLUS405-37/-45

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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